



# ITTEST

## QUESTION & ANSWER

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**Exam : EN0-001**

**Title : ARM Accredited engineer**

**Version : DEMO**

1.In a Cortex-A9 processor, when the Memory Management Unit (MMU) is disabled, which of the following statements is TRUE? (VA is the virtual address and PA is the physical address)

- A.VA == PA; No address translations; instructions and data are not cached
- B.VA! = PA; No address translations; instructions may be cached but not data
- C.VA == PA; Address translations take place; data may be cached but not instructions
- D.VA == PA; No address translations; instructions may be cached but not data

**Answer: D**

2.In the Generic Interrupt Controller (GIC), when an interrupt is requested, but is not yet being handled, it is in which of the following states?

- A.Inactive
- B.Active
- C.Pending
- D.Edge-triggered

**Answer: C**

3.A simple system comprises of the following memory map:

Flash - 0x0 to 0x7FFF

RAM - 0x10000 to 0x17FFF

When conforming to the ABI, which of the following is a suitable initial value for the stack pointer?

- A.Top address of RAM (0x18000)
- B.Top address of flash (0x8000)
- C.Bottom address of RAM (0x10000)
- D.Bottom address of flash (0x0000)

**Answer: A**

4.A program running on a development board that is connected to a host using a debugger can access a file on the host by using:

- A.Memory mapping
- B.Semihosting
- C.Polling
- D.Virtual I/O

**Answer: B**

5.In which type of storage will the compiler preferentially place frequently accessed variables?

- A.Stack
- B.Heap
- C.Registers
- D.Hard disk

**Answer: C**

6.What view in a debugger displays the order in which functions were called?

- A.The Call Stack view
- B.The Memory view

C.The Registers view

D.The Variables view

**Answer: A**

7.Printf statements could be used to achieve which of the following debug tasks?

A.Observe changes to a local variable in a function

B.Capture a real-time trace of program execution

C.Debug boot code, before a call to the C main() function

D.Stop the processor at an interesting location in the code

**Answer: A**

8.When the processor is executing in Thumb state, which of the following statements is correct about the values stored in R15?

A.Bits[31:16] are duplicated with bits[15:0]

B.The PC value is stored in bits[31:1] and bit[0] is treated as zero

C.The PC value is stored in bits[31:16] and bits[15:0] are undefined

D.The PC value is stored in bits[15:0] and bits[31:16] are undefined

**Answer: B**

9.A standard performance benchmark is being run on a single core ARM v7-A processor.The performance results reported are significantly lower than expected.Which of the following options is a possible explanation?

A.L1 Caches and branch prediction are disabled

B.The Embedded Trace Macrocell (ETM) is disabled

C.The Memory Management Unit (MMU) is enabled

D.The Snoop Control Unit (SCU) is disabled

**Answer: A**

10.When setting the initial location of the stack pointer and the base address of the heap, the ARM EABI requires that the:

A.Base address of the heap must be the same as the initial stack pointer.

B.Stack pointer must be 8-byte aligned.

C.Heap must be in external RAM.

D.Initial stack pointer must be the lowest addressable memory location.

**Answer: B**

11.In an ARMv7-A processor, which control register is used to enable the Memory Management Unit (MMU)?

A.The ACTLR

B.The SCTLR

C.The TTBCR

D.The CONTEXTIDR

**Answer: B**

12.A simple method of measuring the performance of an application is to record the execution time using the clock on the wall or a wristwatch.

When is this method INAPPROPRIATE?

- A.When executing the software using a simulation model
- B.When the processor is a Cortex-R4
- C.When instruction tracing is enabled
- D.When the processor is not executing instructions from cache

**Answer: A**

13.Consider the following code sequence, executing on a processor which implements ARM Architecture v7-A.

LDR r0, [r1]

STR r0, [r2]

STR r3, [r3]

R1 points to a location in normal memory.R2 and R3 point to device memory.

Which of the following statements best describes the ordering rules which apply to this sequence?

- A.The two writes to device memory will happen in program order, but the read can be performed out of order
- B.The memory accesses can happen in any order
- C.The memory accesses will happen in program order
- D.The read to r0 and the write from r0 will happen in program order, but the write from r3 can be performed out of order

**Answer: C**

14.When using the default ARM tool-chain libraries for bare-metal applications.I/O functionality is rerouted and handled by a connected debugger.This is often referred to as semihosting.Which one of the following explanations BEST describes how this feature can be implemented by a debugger?

- A.The library directly sends I/O requests to the debugger using the JTAG connection
- B.While the target is running, the debugger processes I/O requests from a shared queue in memory
- C.The I/O library calls rely on an Ethernet connection to redirect the requests to the debugger
- D.The I/O library calls generate an exception that is trapped and handled by the debugger

**Answer: D**

15.The Cortex-A9 processor implements a feature called "small loop mode" which reduces power consumption when executing small loops by turning off instruction cache accesses.Which of the following statements describes a condition that must be satisfied for this mode to be enabled?

- A.The loop must fit into two cache lines
- B.The loop must only contain forward branches
- C.Only integer arithmetic can be used
- D.All variables must be held in registers

**Answer: A**

16.Which is the best power saving mode to use while waiting to obtain a lock on a semaphore?

- A.Dormant

- B.Standby
- C.Shutdown
- D.Deep sleep

**Answer: B**

17.Which privileged mode can kernel code use to get direct access to the User mode registers R13 and R14?

- A.Abort mode
- B.System mode
- C.Hypeivisor mode
- D.Supervisor mode

**Answer: B**

18.An Advanced SIMD intrinsic has the prototype:

```
int16x4_t vmul_n_s16(int16x4_t a, int16_t b);
```

How many multiplications does this intrinsic compute?

- A.1 multiplication
- B.4 multiplications
- C.16 multiplications
- D.64 multiplications

**Answer: B**

19.Which of the following memory attributes, specified in a translation table entry, could be used to protect a page containing a read-sensitive peripheral from speculative instruction fetches?

- A.S (Secure)
- B.nG (non-Global)
- C.xN (Execute Never)
- D.AP (Access Permission)

**Answer: C**

20.An ARMv7 implementation might include the VFPv4-D32 floating point extension.What does the '32' indicate?

- A.The width of the datapath in bits
- B.The number of double precision floating point registers implemented
- C.The number of bits of data that can be loaded or stored at once
- D.The number of integer operations that can be performed simultaneously

**Answer: B**